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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/499,720	02/08/2000	Dale C. Morris	10991915-1	1658

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EXAMINER	
ROJAS, MIDYS	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/499,720	MORRIS ET AL.	
	Examiner	Art Unit	
	Midys Rojas	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

In view of Applicant's arguments, received on January 25th, 2006, the rejection of claims 1 and 12 under 112 second paragraph has been withdrawn.

Response to Arguments

1. Applicant's arguments, received on January 25th, 2006, with respect to original claims 1-24 have been fully considered but they are not persuasive.

Applicant argues that the Arora patent does not teach the claim 1 limitations of reading a stored previous privilege level state and comparing the read previous privilege level state to the current privilege level since in the Arora patent a previous privilege level state is not stored and therefore cannot be read. However, the Examiner would like to point out that the previous privilege level state is stored in CPL 38 since, as agreed by applicant in his arguments (page 9, paragraph 3), a **prior** instruction would have set the CPL 38 to the proper privilege level and the CPL is maintained (stored) in the processor's register set.

Applicant also argues that the privilege level of the EPC instruction does not teach or suggest the current privilege level. Rather, the EPC instruction directs the processor to change the privilege level of the CPL and provides a future privilege level, not the current privilege level. Applicant notes that the CPL, however, is the current privilege level, not the previous privilege level state, and the privilege level of the EPC instruction is a future privilege level, not the current privilege level as submitted by the examiner. However, the privilege level of EPC is the privilege level necessary for the instruction that is currently being prepared for execution in the system, thus it is a current privilege level. The CPL is the previous privilege level because it

was the privilege level necessary for the execution of a previous instruction. Therefore, Arora does teach comparing the read previous privilege level state to the current privilege level.

Applicant argues that there is not reaching or suggestion to combine the Aurora Patent with the Mattison publication. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Arora to restrict access to memory as done by Mattison thus allowing the system to only allow authorized modifications to memory (motivation provided by Mattison, paragraph 0014).

Applicant also argues that is directed to a method and apparatus for protecting flash memories and it is not related to pipeline instructions or privilege levels. In response to applicant's argument that the Mattison publication is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Mattison relates to memory systems which is indeed in applicant's field of endeavor since applicant's system has memories.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arora (6,393,556) in view of Mattison (US 2002/0069316).

Regarding Claims 1 and 6, Arora discloses a method of promoting a current privilege level ("change current privilege level to a higher privilege level" Column 6, lines 46-61) wherein the current privilege level controls application instruction execution in the system by controlling accessibility to the system resources (Column 1, lines 30-41), the method comprising: performing a privilege level promotion instruction by the operating system (Column 4, lines 13-27, and Column 6, lines 46-61), the privilege promotion instruction being stored in a first page of memory (instruction memory 36 storing a plurality of instructions... see Figure 2) wherein processing these instructions direct the processor to change the privilege level (privilege promotion instructions, see Col. 2, lines 19- 37), the privilege promotion instruction including: reading a stored previous privilege level state,

comparing the read previous privilege level state (CPL 38) to the current privilege level (comparing the current privilege level to the instruction's privilege level wherein this case the instruction's privilege level is the current privilege level and the stored privilege level is the previous privilege level, column 6, lines 46-49. The privilege level stored in CPL 38 is the

previous privilege level since it represents a previous instruction, while the privilege level related to the EPC is the current privilege level since it represents the current instruction),

and if the previous privilege level state is equal to or less privileged than the current privilege level (since the EPC instruction directs the processor to change the architectural privilege level to a higher privilege level..."), promoting the current privilege level to a second privilege level which is higher than the first privilege level ("...increase the architectural current privilege level from privilege level 3 to privilege level 0"). In comparing privilege levels, it is understood that the stored privilege level (stored in CPL 38) must be read in the comparison process.

Arora discloses processing "branch" instructions (Col. 3, lines 55-67) and "return" instructions instructing the program to return from a subroutine, wherein branch and return instructions need return addresses for returning from a particular branch. Branch instructions involve altering the program path by branching to a subroutine in a particular branch address and returning to the original program path using a stored return address.

Arora does not teach storing the privilege level promotion instruction in a page of memory not writable by application instructions at a first privilege level. Mattison discloses restricting processor access to instructions stored in main memory when in a particular mode of operation (in this case main memory is not writable by the processor and this particular mode of operation represents the processor's privilege level, paragraphs 0015-0016). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Arora to restrict access to memory as done by Mattison thus allowing the system to only allow authorized modifications to memory (Mattison, paragraph 0014).

Regarding Claims 12, 17 and 23 Arora discloses a computer system comprising a processor (Figure 2, processor 30) having current privilege level which controls accessibility to the system resources (Column 1, lines 30-41 and Column 4, lines 13-16', see Figure 2, CPL 38) and having a previous privilege level state ("second privilege level", Column 6, lines 27-32)', a memory (Figure 2, Instruction memory 36) having a plurality of memory pages including a first memory page storing a privilege promotion instruction ("memory stores a plurality of instructions" such as an "EPC instruction which directs the processor to change the privilege level of the architectural current privilege level", see Column 3, lines 20-25 and Column 4, lines 13-27), and performing the privilege level promotion instruction as follows:

reading a stored previous privilege level state,

comparing the read previous privilege level state (stored in CPL 38) to the current privilege level (comparing the stored current privilege level to the instructions privilege level wherein this case the instruction's privilege level is the current privilege level and the stored privilege level is the previous privilege level, column 6, lines 46-49, column 6, lines 46-49),

and if the previous privilege level state (stored in CPL 38) is equal to or less privileged than the current privilege level ("since the EPC instruction directs the processor to change the architectural privilege level to a higher privilege level...", promoting the current privilege level to a second privilege level which is higher than the first privilege level ("...increase the architectural current privilege level from privilege level 3 to privilege level 0"). In comparing privilege levels, it is understood that the stored privilege level must be read in the comparison process.

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instructions need return addresses for returning from a particular branch. Branch instructions involve altering the program path by branching to a subroutine in a particular branch address and returning to the original program path using a stored return address.

Arora does not teach storing the privilege level promotion instruction in a page of memory not writable by application instructions at a first privilege level. Mattison discloses restricting processor access to instructions stored in main memory when in a particular mode of operation (in this case main memory is not writable by the processor and this particular mode of operation represents the processor's privilege level, paragraphs 0015-0016). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Arora to restrict access to memory as done by Mattison thus allowing the system to only allow authorized modifications to memory (Mattison, paragraph 0014).

Regarding Claims 2, 8, 13, and 19, Arora discloses the method of promoting a current privilege level wherein the step of performing the privilege promotion instruction further includes: if the previous privilege level state is more privileged then the current privilege level ("if the EPC instruction specifies a privilege level lower than or the same as the architectural current privilege level..."), taking an illegal operation fault ("the processor will issue a fault", Column 6, lines 55-61).

Regarding Claims 3, 9, 14, and 20, Arora discloses the method of promoting a current privilege level wherein the system resources include system registers (architectural register set, Column 3, lines 61-67).

Regarding Claims 4, 10, 15, and 21, Arora discloses the method of promoting a current privilege level wherein the system resources include system instructions ("memory 36 stores a plurality of instructions that are processed in the pipeline", column 3, lines 22-25).

Regarding Claims 5, 11, 16, and 22, Arora discloses the method of promoting a current privilege level wherein the system resources include memory pages (Figure 2, instruction memory 36).

Regarding Claim 7, 18, and 24 Arora discloses the method of promoting a current privilege level further comprising: performing a return instruction including: transferring instruction control flow to the stored return address to the first page of memory ("a return instruction would instruct the processor to decrease the architectural current privilege level to the previous privilege level", Column 6, line 65-Column 7, line 3), and demoting the current privilege level to the stored previous privilege level.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 28, 2006

Midys Rojas
Midys Rojas
Examiner
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MR

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